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July 31, 2000

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

VIA EXPRESS MAIL NO. EL417461943US

Re: Patent Application for "Wafer/Interposer Assembly Apparatus and Method"
Inventor: Jerry D. Kline
Our File No.: 121251-1004

Dear Sir:

Enclosed for filing in connection with the above-referenced U.S. patent application, please find the following:

(1) Patent Application (37 pages plus 8 sheets of informal drawings);
(2) Fee Calculation Sheet; and
(3) Return Postcard.

Please file the above documents and return the file-stamped postcard to our offices. The Commissioner is hereby authorized to charge the filing fee of $552.00 and any additional fees which may be required by this paper to Deposit Account No. 07-0153.

Thank you for your assistance. Should you have any questions, please call me.

Respectfully submitted,

GARDERE & WYNNE, L.L.P.

Daniel J. Chalker
Registration No. 40,552

DJC/hrh

Enclosures
cc: Sanford E. Warren, Jr.

896181.1

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APPLICATION FOR U.S. PATENT
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Attorney Docket No.: 121251-1004

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Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): Jerry D. Kline of Argyle, Texas

For: "Wafer/Interposer Assembly Apparatus and Method"

Enclosed are: 8 Sheet(s) of informal drawings;
27 pages of Specification;
9 pages of Claims; and
1 page of Abstract.

FEE CALCULATION					FEE
	NUMBER		**NUMBER EXTRA**	**RATE**	**BASIC FEE $ 345.00**
Total Claims	43	-20 =	23	x$ 9 =	$ 207.00
Independent Claims	3	- 3 =	0	x$ 39=	$ 0.00
				Total Filing Fee	$ 552.00

The Commissioner is hereby authorized to charge the filing fee of $552.00 and any additional fees which may be required, or credit any overpayment to Deposit Account No. 07-0153. **This form is submitted in duplicate.**

All correspondence related to this application may be addressed to the undersigned at:
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Date: July 31, 2000

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G&W No. 121251-1004 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

WAFER-INTERPOSER ASSEMBLY APPARATUS AND METHOD

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VIA EXPRESS MAIL EL417461943US ON 7/31/2000

WAFER-INTERPOSER ASSEMBLY TEST APPARATUS AND METHOD

FIELD OF THE INVENTION

The present invention relates generally to the field of integrated circuits, and more particularly, to a wafer-interposer assembly apparatus and method.

BACKGROUND OF THE INVENTION

Semiconductor die have traditionally been electrically connected to a package by wire bonding techniques, in which wires are attached to pads of the die and to pads located in the cavity of the plastic or ceramic package. Wire bonding is still the interconnection strategy most often used in the semiconductor industry today. But the growing demand for products that are smaller, faster, less expensive, more reliable and have a reduced thermal profile has pushed wire bonding technology to its limits (and beyond) thereby creating barriers to sustained product improvement and growth.

The high-performance alternative to wire bonding techniques are flip chip techniques, in which solder balls or bumps are attached to the input/output (I/O) pads of the die at the wafer level. The bumped die is flipped over and attached to a substrate "face down," rather than "face up" as with wire bonding. Flip chips resolve many if not all of the problems introduced by wire bonding. First, flip chips have fewer electrical interconnects than wire bonding, which results in improved reliability and fewer manufacturing steps, thereby reducing production costs. Second, the face down mounting of a flip chip die on a substrate allows superior thermal management techniques to be deployed than those available in wire bonding. Third, flip chips allow I/O to be located essentially anywhere on the die, within the limits of substrate pitch technology and manufacturing equipment, instead of forcing I/O to the peripheral of the die as in wire bonding. This results in increased I/O density and system miniaturization.

Despite the advantages of the flip chip, wide spread commercial acceptance of the flip chip has been hindered by testing issues. To ensure proper performance, the die should be adequately tested before it is assembled into a product; otherwise, manufacturing yields at the module and system level can suffer and be unacceptably low. Under some circumstances, a defective die can force an entire subassembly to be scrapped. One attempt to address this testing issue has been to perform a wafer probe, followed by dicing the wafer and temporarily packaging each die into a test fixture of some sort. Performance testing is subsequently executed. Burn-in testing is often included in this process to eliminate any die having manufacturing process defects. Following the successful completion of these tests, the die are removed from the test fixture and either retailed as a Known Good Die ("KGD") product or used by the manufacturer in an end product, such as a Multichip Module ("MCM"). The Multichip Module may constitute a subassembly in a larger system product. This Known Good Die process is inherently inefficient due to its complexity.

Accordingly, there is a need for a wafer-interposer assembly apparatus and method that is simple, allows testing at the wafer level before dicing, and eliminates the need for temporarily packaging the die in a carrier.

SUMMARY OF THE INVENTION

The present invention provides a wafer-interposer assembly apparatus and method that is simple, allows testing at the wafer level before dicing, and eliminates the need for temporarily packaging the die in a carrier. As a result, the number of manufacturing operations are reduced, thereby improving first pass yields. In addition, manufacturing time is decreased, thereby improving cycle times and avoiding additional costs.

More specifically, the present invention provides several possible test systems, apparatus and method of interfacing multiple semiconductor wafer to the testing equipment through the use of interposer assemblies, which enhances economies of scale. The interposer revolutionizes the semiconductor fabrication process enabling testing and burn-in of all die at the wafer level. For example, the interposer eliminates the need to singulate, package, test, then unpackage each die individually to arrive at a Known Good Die product stage. Furthermore, the interposer may remain attached to the die following dicing, thereby providing the additional benefit of redistributing the die I/O pads to a standard Joint Electrical Dimensional Electronic Committee ("JDEC") interconnect pattern for Direct Chip Attachment ("DCA") applications.

The present invention provides a method for manufacturing a wafer-interposer assembly including the steps of providing a semiconductor wafer and an interposer. The semiconductor wafer including one or more semiconductor die, each semiconductor die having one or more first electrical contact pads. The interposer having one or more communication interfaces and a second electrical contact pad corresponding to each of the

one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, and at least one of the second electrical contact pads electrically connected to the one or more communication interfaces. The wafer-interposer assembly is formed by connecting each first electrical contact pad of the semiconductor wafer to the corresponding second electrical contact pad of the interposer with a conductive attachment element.

The present invention also provides a wafer-interposer assembly having an interposer connected to a semiconductor wafer. The semiconductor wafer includes one or more semiconductor die, each semiconductor die having one or more first electrical contact pads. The interposer includes one or more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, at least one of the second electrical contact pads electrically connected to the one or more communication interfaces, and each first electrical contact pad of the semiconductor wafer connected to the corresponding second electrical contact pad of the interposer with a conductive attachment element.

In addition, the present invention provides an interposer having a multi-layer sheet having a first surface and a second surface, a first pattern of electrical contact pads disposed on the first surface, one or more communication interfaces and a set of conductors. The first pattern of electrical contact pads correspond to a second pattern of electrical contact pads disposed on a surface of a semiconductor wafer. The one or more communication interfaces are attached to the multi-layer sheet. The set of conductors each of which connect at least

one electrical contact pad disposed on the first surface to the one more communication interfaces.

Moreover, the present invention provides wafer-interposer assemblies having various types of communication interfaces, such as integral edge connector(s) with pins and/or sockets, integral bayonet connector(s) with pins and/or sockets, one or more connectors added to the wafer-interposer assembly, one or more soldered connections, one or more ribbon connectors, one or more RF connectors, one or more optical or infrared connectors, one or more transmit/receive antennas, or one or more clamps or quick release devices.

Other features and advantages of the present invention shall be apparent to those of ordinary skill in the art upon reference to the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further advantages of the invention may be better understood by referring to the following description in conjunction with the accompanying drawings in which corresponding numerals in the different figures refer to corresponding parts in which:

FIGURE 1 is an exploded view of a wafer-interposer assembly in accordance with one embodiment of the present invention;

FIGURE 2 is a cross-sectional view of an interposer in accordance with one embodiment of the present invention;

FIGURE 3 is a perspective view of a wafer-interposer assembly being inserted into a testing apparatus in accordance with one embodiment of the present invention;

FIGURE 4 is a perspective view of a wafer-interposer assembly having integral edge connector(s) with pins and/or sockets in accordance with one embodiment of the present invention;

FIGURE 5 is a perspective view of a wafer-interposer assembly having integral bayonet connector(s) with pins and/or sockets in accordance with one embodiment of the present invention;

FIGURE 6 is a perspective view of a wafer-interposer assembly having one or more connectors added to the wafer-interposer assembly in accordance with one embodiment of the present invention;

FIGURE 7 is a perspective view of a wafer-interposer assembly having one or more connectors added to the wafer-interposer assembly in accordance with one embodiment of the present invention;

FIGURE 8 is a perspective view of a wafer-interposer assembly having one or more soldered connections in accordance with one embodiment of the present invention;

FIGURE 9 is a perspective view of a wafer-interposer assembly having one or more ribbon connectors in accordance with one embodiment of the present invention;

FIGURE 10 is a perspective view of a wafer-interposer assembly having one or more RF connectors in accordance with one embodiment of the present invention;

FIGURE 11 is a perspective view of a wafer-interposer assembly having one or more optical or infrared connectors in accordance with one embodiment of the present invention;

FIGURE 12 is a perspective view of a wafer-interposer assembly having one or more transmit/receive antennas in accordance with one embodiment of the present invention;

FIGURE 13 is a perspective view of a wafer-interposer assembly having one or more clamps or quick release devices in accordance with one embodiment of the present invention;

FIGURE 14 is an exploded view of a wafer-interposer assembly having an array of conductive attachment elements disposed on the upper surface thereof in accordance with the present invention;

FIGURE 15 is an isometric view of multiple chip assemblies after singulation of the wafer-interposer assembly in accordance with the present invention; and

FIGURE 16 is an isometric view of a chip assembly in place on a substrate in accordance with the present invention.

DETAILED DESCRIPTION

While the making and using of various embodiments of the present invention are discussed herein in terms of a wafer-interposer assembly testing apparatus and method, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and does not limit the scope of the invention.

The present invention provides a wafer-interposer assembly apparatus and method that is simple, allows testing at the wafer level before dicing, eliminates the need for temporarily packaging the die in a carrier, and allows for simultaneous or near simultaneous testing multiple wafer-interposer assemblies. As a result, the number of manufacturing operations are reduced, thereby improving first pass yields. In addition, manufacturing time is decreased, thereby improving cycle times and avoiding additional costs.

Moreover, the interposer revolutionizes the semiconductor fabrication process enabling testing and burn-in of all die at the wafer level. For example, the interposer eliminates the need to singulate, package, test, then unpackage each die individually to arrive at a Known Good Die product stage. This results in a significant cost avoidance opportunity for wafer manufacturers. Furthermore, the interposer may remain attached to the die following dicing, thereby providing the additional benefit of redistributing the die I/O pads to a standard Joint Electrical Dimensional Electronic Committee ("JDEC") interconnect pattern for Direct Chip Attachment ("DCA") applications.

The general features of a wafer-interposer assembly, generally designated 10, in accordance with the present invention are shown in FIGURE 1. A wafer-interposer assembly 10 comprises a wafer 12 having one or more chips 14 therein. Wafer 12 is depicted as having eighteen chips 14 for simplicity that are separated by dashed lines for clarity. Each chip 14 has one or more conductive pads 16 on its surface. For each chip 14 there is a corresponding array 18 of conductive attachment elements 20 one for each conductive pad 16. The conductive attachment elements 20 may be solder balls or bumps, screened solder paste, a set of conductive two part or heat cured epoxy, conductive thermoplastic balls or bumps or other electrical connection methods known in the art.

In one embodiment, the interposer 22 has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In another embodiment, the interposer does not have the array 24 of conductive pads 26. Instead, all conductors 32, 34, 36 and 38 (FIGURE 2) are routed to the one or more communication interfaces, which are described in this embodiment as socket 30 in connector 28. In such a case, elements 24 and 26 in FIGURES 1 and 3 through 13 are not required. The interposer 22 also has an array of conductive pads (not shown) on the surface facing the wafer 12, one for each conductive pad 16 on the surface of the wafer 12. After assembly, the conductive attachment elements 20 electrically connect and mechanically bond the pads 16 of each chip 14 to the facing interposer pads (not shown).

The interposer 22 is preferably directly and permanently attached to the wafer 12, thereby eliminating the wafer-bumping step currently required for Flip chip and Flip

chip/DCA applications. Alternately, the interposer 22 may be created by application of materials on the wafer 12 itself, such as ink jet deposition of conductive epoxy, solder or polyimide. These materials can also be rolled on, sprayed on or applied through stereolithographic technologies. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the interposer 22.

As best seen in FIGURE 2, interposer 22 includes one or more layers having etched routing lines and vias therein which serve as electrical conductors. One set of conductors, depicted as conductors 32 and 34 pass through the interposer 22 to electrically connect the pads 16 on the chips 14 to the pads of a substrate to which the chip assembly will be attached as explained in more detail below. Conductors 32 and 34 are selected to have suitable conductivity and may be, for example, copper.

Testing conductors, depicted as conductors 36 and 38 pass through the interposer 22 connecting the pads 16 of the chips 14 to the testing sockets 30 in the testing connector 28, as best seen in FIGURE 1. The testing conductors 36 and 38 may provide direct electrical connection between the testing sockets 30 and the pads 16, or may pass through a multiplexer or other intervening apparatus (not shown) incorporated into the interposer 22. As a result, the interposer 22 electrically connects all relevant nodes to standard test equipment without the need for probes.

Assembly of the wafer 12 and interposer 22 is accomplished through creating a set of permanent electrical and mechanical connections between the wafer 12 and interposer 22 using the conductive attachment elements 20. The conductive attachment elements 20 will typically be implemented as features on both the upper and lower surfaces of the interposer 22 but may alternatively be placed on the wafer 12. Likewise, the attachment elements 20 could be incorporated into a sheet or similar structure sandwiched between the wafer 12 and interposer 22 during assembly.

In order to test the chips 14 using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 on each chip 14 through the testing connector 28. For a wafer 12 having a substantial number of chips 14, each having a large number of pads 16, it may be desirable to connect the pads 16 to the testing sockets 30 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14. Such a design removes the necessity for a dedicated testing socket 30 for each chip pad 16, thereby reducing the complexity of the testing connector 28.

While FIGURE 1 depicts an interposer 22 having a single, rectangular testing connector 28, it should be understood by those skilled in the art that interposer 22 could be attached to a testing apparatus in a variety of ways. For example, interposer 22 may have multiple testing connectors having various sizes, shapes and numbers of sockets. Likewise,

interposer 22 may alternatively have testing connectors mounted on the top surface thereof instead of or in addition to the side mounted testing connectors or may use cables for connection to a testing apparatus.

It should also be noted that interposer 22 may include bypass capacitors to minimize ground bounce and to filter bias voltage. These capacitors may be standard surface mount devices or embedded within interposer 22. Additionally, interposer 22 may include inductors to provide additional filtering. Impedance matching networks and line drivers may also be incorporated into interposer 22 to ensure signal integrity and to accurately measure parameters such as signal rise time and bandwidth and to protect the semiconductor chips 14 in the event of test equipment failure.

The pads 26 on the upwardly facing surface of interposer 22 are depicted in FIGURE 1 having the identical geometry as the pads 16 of the chips 14 of the wafer 12. The invention herein disclosed is by no means limited to this geometry. As each die design may have unique pad geometry, one of the advantages of the present invention is that pads 26 of interposer 22 may utilize a geometry that is different than that of the chips 14. Traditionally, chip designers were limited in chip layout in that all connections between the elements of the chip 14 and the outside world had to be made either through the peripheral edges of the chip (for wire bonding) or at least through a standard pin or pad layout defined by a standardization body, such as the Joint Electrical Dimensional Electronic Committee (JEDEC). The interconnection requirements, therefore, have traditionally driven the chip layout.

Through the use of the interposer 22, the layout of a chip 14 and its pads 16 can be defined according to the interaction of the functional elements of the chip 14 rather than according to the standardization requirements. The interposer 22 can be designed with a standardized layout of pads 26 on its upper surface and can electrically connect each chip pad 16 to the corresponding upper interposer pad 26 without an interposer pad 26 being directly above its corresponding chip pad 16. Not only does the interposer 22 of the present invention provide for standardized interconnection, it also provides for the use of standard test hardware, software, cabling and connectors compatible with existing industry infrastructure.

An additional advantage of interposer 22 of the present invention is that more than one interposer 22 can be designed for each wafer 12. A manufacturer can then, by substituting a different interposer 22, modify the layout of the output pads 16 to conform to a different layout or packaging standard. Alternatively, if the chip 14 and interposer 22 are designed for modularity, a single interposer design may be useful on more than one chip design. A specific interposer design will typically be necessary for each unique wafer design.

Turning now to FIGURE 3, a wafer 12 and interposer 22 are shown as an assembly 40 ready to be connected to a testing unit 46 in accordance with the present invention. The wafer-interposer assembly 40 interfaces to the testing unit 46 through a testing connector 42 comprising one or more testing contacts 44, shown here as pins. The testing contacts 44 in the testing connector 42 connect with the testing contacts 30 (FIGURE 1) of the interposer 22. As noted above, the testing connector 42 need not incorporate a testing contact 44 for

every chip pad. The contacts 44 may connect to the chips through a multiplexer or similar device (not shown). In addition, the testing connector 42 may be keyed to the shape of the wafer-interposer assembly 40 so that the wafer-interposer assembly 40 cannot be incorrectly inserted into the testing connector 42.

After electrical connection to the testing unit 46, the wafer-interposer assembly 40 can be run through a complete parametric test or whatever subset thereof is deemed necessary for that particular chip design. During the course of testing, each function of the chip may ideally be tested across a range of conditions, so as to simulate real world operation. The testing unit 46 may incorporate a heating and cooling apparatus for testing the chips across a range of temperatures. The testing unit 46 may also incorporate a device for vibrating or otherwise mechanically stressing the chips 14. During testing, non-conforming chips are identified by the testing unit 46 such that they may be discarded after singulation of the wafer-interposer assembly 40. Alternatively, where a manufacturer sells a variety of grades of a particular model of chip, individual chips can be graded according to various performance criteria, such as maximum clock speed or thermal stability, for later classification and sorting. Such parametric data and attribute data are stored by the testing unit 46 and may be displayed or printed for the operator. Other information such as operator identification code, date, lot number and the like will be stored.

While FIGURE 3 depicts a single wafer-interposer assembly 40 being tested, multiple wafer-interposer assemblies may be tested in a rack and/or bank configuration. It should be understood by those skilled in the art that groups of wafer-interposer assemblies

could be tested using other topologies. In such a testing scenarios, additional multiplexers, capacitor, impedance matching networks and related components would typically be used.

FIGURES 4 through 13 will now depict various embodiments of one or more communication interfaces that may be used for testing and/or operational use of the semiconductor wafer and/or die. Now referring to FIGURE 4, a wafer-interposer assembly 50 having integral edge connector(s) 52 with pins and/or sockets in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 50 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the testing connector 28. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the integral edge connector(s) 52, which may include pins and/or sockets, through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a dedicated integral edge connector(s) 52 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the testing connector 28.

Referring to FIGURE 5, a wafer-interposer assembly 54 having integral bayonet connector(s) 56 with pins and/or sockets in accordance with one embodiment of the present invention is shown. The integral bayonet connector(s) 56 may extend vertically upward as shown or vertically downward (not shown). As previously described, the wafer-interposer assembly 54 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the testing connector 28. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the integral bayonet connector(s) 56, which may include pins and/or sockets, through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a dedicated integral bayonet connector(s) 56 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the testing connector 28.

Now referring to FIGURE 6, a wafer-interposer assembly 58 having one or more connectors 62 added to the wafer-interposer assembly 58 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 58 includes an interposer 60 attached to a wafer 12. In order to test the

chips 14 (FIGURE 1) using the interposer 60, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the one or more connectors 62. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more connectors 62 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 60 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a dedicated pins or sockets within the one or more connectors 62 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the one or more connectors 62.

Referring now to FIGURE 7, a wafer-interposer assembly 64 having one or more connectors 68 added to the wafer-interposer assembly 64 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 64 includes an interposer 66 attached to a wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 66, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the one or more connectors 68. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more connectors 68 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 66 as a standard

surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a dedicated pins or sockets within the one or more connectors 68 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the one or more connectors 68.

Now referring to FIGURE 8, a wafer-interposer assembly 70 having one or more soldered connections 72 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 70 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the testing connector 28. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more soldered connections 72 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a soldered connection 72 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the testing connector 28.

Referring now to FIGURE 9, a wafer-interposer assembly 74 having one or more ribbon connectors 76 in accordance with one embodiment of the present invention is shown. Alternatively, the ribbon connectors 76 may extend from other surfaces of the wafer-interposer assembly 74. As previously described, the wafer-interposer assembly 74 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the testing connector 28. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more ribbon connectors 76 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a lead within the ribbon connector 76 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the testing connector 28.

Now referring to FIGURE 10, a wafer-interposer assembly 78 having one or more RF connectors 80 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 78 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the

surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the testing connector 28. A cut away drawing of the testing connector 28 is depicted and labeled as 79, and shows a detail of a RF connector 80 as it can be connected to a testing cable connector 81. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more RF connectors 80 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for an RF connector 80 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the testing connector 28.

Referring now to FIGURE 11, a wafer-interposer assembly 82 having one or more optical or infrared connectors 84 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 82 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) via the one or more optical or infrared connectors 84. For a wafer 12 having a substantial number of chips 14

(FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more optical or infrared connectors 84 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for an optical or infrared connector 84 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the interposer 22. Alternatively, the optical or infrared connectors 84 can be located in connector assembly 28.

Now referring to FIGURE 12, a wafer-interposer assembly 86 having one or more transmit/receive antennas 88 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 86 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the testing connector 28. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the transmit/receive antennas 88 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test

apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for an transmit/receive antennas 88 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the transmit/receive antennas 88.

Referring now to FIGURE 13, a wafer-interposer assembly 90 having one or more clamps or quick release devices 92 in accordance with one embodiment of the present invention is shown. As previously described, the wafer-interposer assembly 90 includes an interposer 22 attached to a wafer 12. In addition, the interposer has an array 24 of conductive pads 26 on the surface facing away from the wafer 12. In order to test the chips 14 (FIGURE 1) using the interposer 22, it will be necessary that a testing apparatus be able to connect to the full array of pads 16 (FIGURE 1) on each chip 14 (FIGURE 1) through the one or more clamps or quick release devices 92. For a wafer 12 having a substantial number of chips 14 (FIGURE 1), each having a large number of pads 16 (FIGURE 1), it may be desirable to connect the pads 16 (FIGURE 1) to the one or more clamps or quick release devices 92 through one or more multiplexers (not shown). The multiplexer could be built into the interposer 22 as a standard surface mount device or could be a separate component or set of components. The multiplexer could be powered by the test apparatus or from the bias voltage powering the semiconductor chips 14 (FIGURE 1). Such a design removes the necessity for a clamp or quick release device 92 for each chip pad 16 (FIGURE 1), thereby reducing the complexity of the interposer 22.

Turning now to FIGURE 14, a wafer-interposer assembly 140 is shown having an array 24 of conductive pads 26 on its upper surface. The array 150 of conductive attachment

elements 152 may typically be attached to interposer 22 prior to its attachment to wafer 12. Alternatively, the conductive attachment elements 152 may not be attached to interposer 22 at all or may be attached to the interposer 22 following testing of chips 14 (FIGURE 1) of wafer 12. The conductive attachment elements 152 may be of the types discussed above with reference to FIGURE 1.

FIGURE 15 shows an array of chip assemblies 162, after singulation of the wafer-interposer assembly 140 (FIGURE 14). Each chip assembly 162 comprises a chip 164, an interposer 166 and a plurality of conductive attachment elements 170 deposited on the conductive pads 168 on the exposed surface of the interposer 166. The chip assemblies 162 will be separated into conforming and non-conforming groups or sorted by performance level according to the results of the wafer level testing described in accordance with FIGURE 3. The wafer-interposer assembly 140 (FIGURE 14) can be singulated into groups of chip assemblies 162 instead of individual die.

FIGURE 16 shows an assembly 180 comprising a chip assembly 162 mounted on a substrate 182 having a plurality of conductive layers 190 and dielectric layers 188. The chip assembly 162 is electrically and mechanically attached to pads 184 on the surface of the substrate 182 through conductive attachment elements 186. The chip assembly 162 communicates with other electronic devices (not shown) through the conductive layers 190 of the substrate 182. Assembled as shown, the interposer 166 provide electrical connection between the chip 164 the substrate 182.

In certain embodiments, the substrate 182 may represent a traditional FR4 circuit board. In other embodiments, the substrate 182 may be composed of a higher grade material suitable for use in multichip modules requiring finer conductor pitch. In the latter embodiment, the chip assembly 162 would generally be one of several such assemblies mounted on a small substrate in close proximity. This invention is well suited for implementation in these assemblies. It can be seen in FIGURE 16 that the chip assembly 162 occupies an area of substrate 182 only slightly larger than the surface of the chip 164. This is in contrast to traditional semiconductor assemblies, in which the area consumed by each chip package is much greater than the area of the chip itself.

While specific alternatives to steps of the invention have been described herein, additional alternatives not specifically disclosed but known in the art are intended to fall within the scope of the invention. For example, any combination and orientation of the connectors illustrated and described above may be used within the scope of the present invention. Thus, it is understood that other applications of the present invention will be apparent to those skilled in the art upon the reading of the described embodiment and a consideration of the appended claims and drawings.

CLAIMS

1. A method for manufacturing a wafer-interposer assembly comprising the steps of:

providing a semiconductor wafer including one or more semiconductor die, each semiconductor die having one or more first electrical contact pads;

providing an interposer having one or more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, and at least one of the second electrical contact pads electrically connected to the one or more communication interfaces; and

forming the wafer-interposer assembly by connecting each first electrical contact pad of the semiconductor wafer to the corresponding second electrical contact pad of the interposer with a conductive attachment element.

2. The method as recited in claim 1, further comprising the steps of:

attaching the wafer-interposer assembly to a testing apparatus; and

testing the semiconductor die.

3. The method as recited in claim 3, further comprising the step of singulating the wafer-interposer assembly into one or more chip assemblies.

4. The method as recited in claim 1 wherein the step of testing the semiconductor die further comprises performing a parametric test of at least one of the semiconductor die.

5. The method as recited in claim 1 wherein the step of testing the semiconductor die further comprises testing the semiconductor die in sequence.

6. The method as recited in claim 1 wherein the step of testing the semiconductor die further comprises testing the semiconductor die simultaneously.

7. The method as recited in claim 1 wherein the step of testing the semiconductor chips further comprises using a multiplexer.

8. The method as recited in claim 1 further comprising the step of grading each of the semiconductor die during testing and sorting the semiconductor chips based upon performance level.

9. The method as recited in claim 1 further comprising the step of grading each of the semiconductor die during testing and sorting the semiconductor die into conforming and non-conforming groups.

10. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more integral edge connectors with pins and/or sockets.

11. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more integral bayonet connectors with pins and/or sockets.

12. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more connectors added to the wafer-interposer assembly.

13. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more soldered connections.

14. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more ribbon connectors.

15. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more RF connectors.

16. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more optical or infrared connectors.

17. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more transmit/receive antennas.

18. The method as recited in claim 1 wherein the one or more communication interfaces comprises one or more clamps or quick release devices.

19. A wafer-interposer assembly comprising:

a semiconductor wafer including one or more semiconductor die, each semiconductor die having one or more first electrical contact pads; and

an interposer connected to the semiconductor wafer, the interposer having one or more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, at least one of the second electrical contact pads electrically connected to the one or more communication interfaces, and each first electrical contact pad of the semiconductor wafer connected to the corresponding second electrical contact pad of the interposer with a conductive attachment element.

20. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more integral edge connectors with pins and/or sockets.

21. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more integral bayonet connectors with pins and/or sockets.

22. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more connectors added to the wafer-interposer assembly.

23. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more soldered connections.

24. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more ribbon connectors.

25. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more RF connectors.

26. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more optical or infrared connectors.

27. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more transmit/receive antennas.

28. The wafer-interposer assembly as recited in claim 19 wherein the one or more communication interfaces comprises one or more clamps or quick release devices.

29. An interposer comprising:

a multi-layer sheet having a first surface and a second surface;

a first pattern of electrical contact pads disposed on the first surface and corresponding to a second pattern of electrical contact pads disposed on a surface of a semiconductor wafer;

one or more communication interfaces attached to the multi-layer sheet; and

a set of conductors each of which connect at least one electrical contact pad disposed on the first surface to the one more communication interfaces.

30. The interposer as recited in claim 29 further comprising a third pattern of electrical contact pads disposed on the second surface of the multi-layer sheet and connected to one or more of the electrical contact pads disposed on the first surface via one or more conductors.

31. The interposer as recited in claim 29 further comprising a multiplexer between the electrical contact pads disposed on the first surface and the one or more communication interfaces.

32. The interposer as recited in claim 29 wherein the second pattern of electrical contact pads conforms to an industry-standard layout.

33. The interposer as recited in claim 29 further comprising an array of conductive attachment elements disposed on the first pattern of electrical contact pads.

34. The interposer as recited in claim 29 further comprising an array of conductive attachment elements disposed on the second pattern of electrical contact pads.

35. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more integral edge connectors with pins and/or sockets.

36. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more integral bayonet connectors with pins and/or sockets.

37. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more connectors added to the wafer-interposer assembly.

38. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more soldered connections.

39. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more ribbon connectors.

40. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more RF connectors.

41. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more optical or infrared connectors.

42. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more transmit/receive antennas.

43. The interposer as recited in claim 29 wherein the one or more communication interfaces comprises one or more clamps or quick release devices.

WAFER-INTERPOSER ASSEMBLY APPARATUS AND METHOD

ABSTRACT

The present invention provides a wafer-interposer assembly apparatus and method. The method for manufacturing the wafer-interposer assembly including the steps of providing a semiconductor wafer and an interposer. The semiconductor wafer including one or more semiconductor die, each semiconductor die having one or more first electrical contact pads. The interposer having one or more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, and at least one of the second electrical contact pads electrically connected to the one or more communication interfaces. The wafer-interposer assembly is formed by connecting each first electrical contact pad of the semiconductor wafer to the corresponding second electrical contact pad of the interposer with a conductive attachment element. The one or more communication interfaces may include integral edge connector(s) with pins and/or sockets, integral bayonet connector(s) with pins and/or sockets, one or more connectors added to the wafer-interposer assembly, one or more soldered connections, one or more ribbon connectors, one or more RF connectors, one or more optical or infrared connectors, one or more transmit/receive antennas, or one or more clamps or quick release devices.

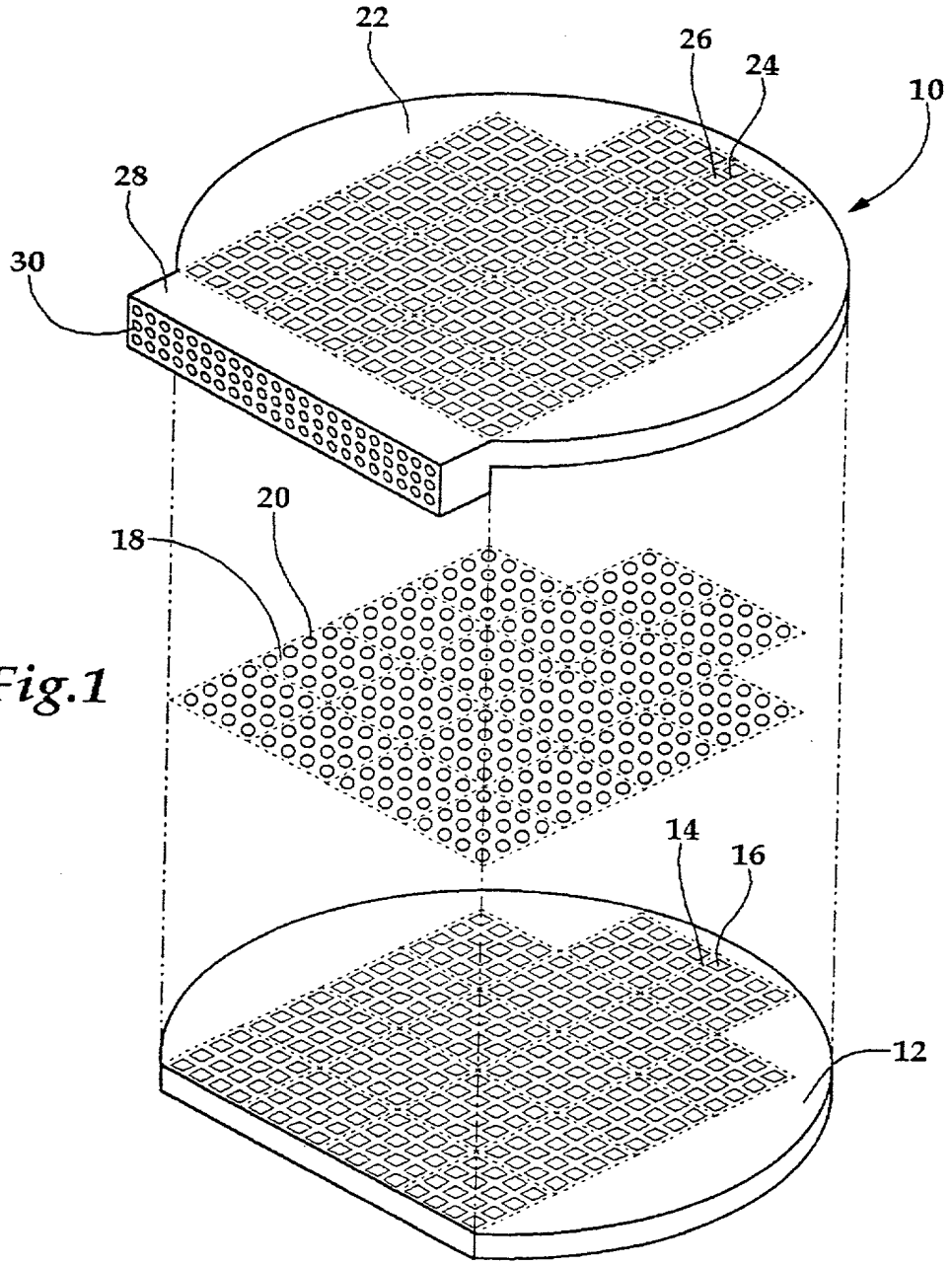

Fig.1

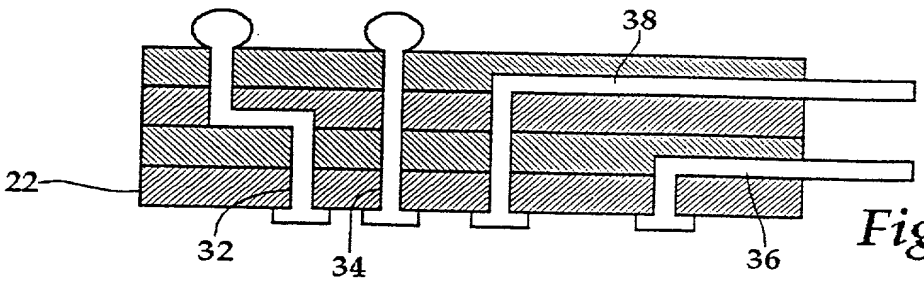

Fig.2

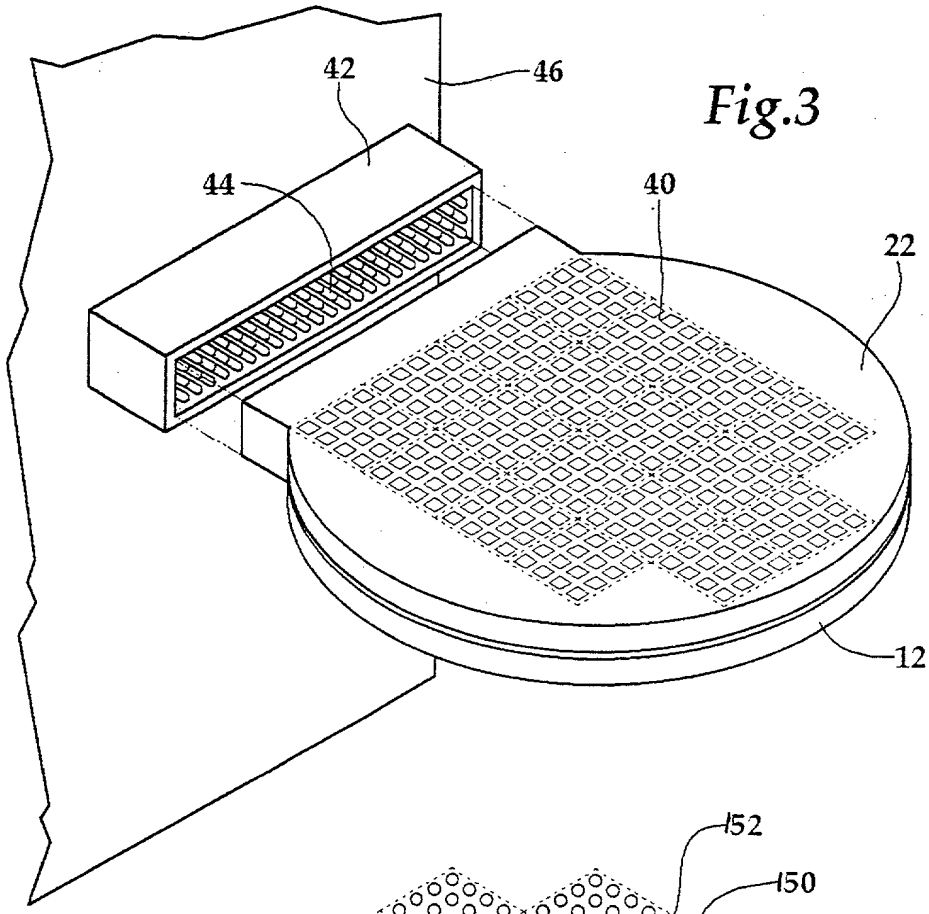

Fig.3

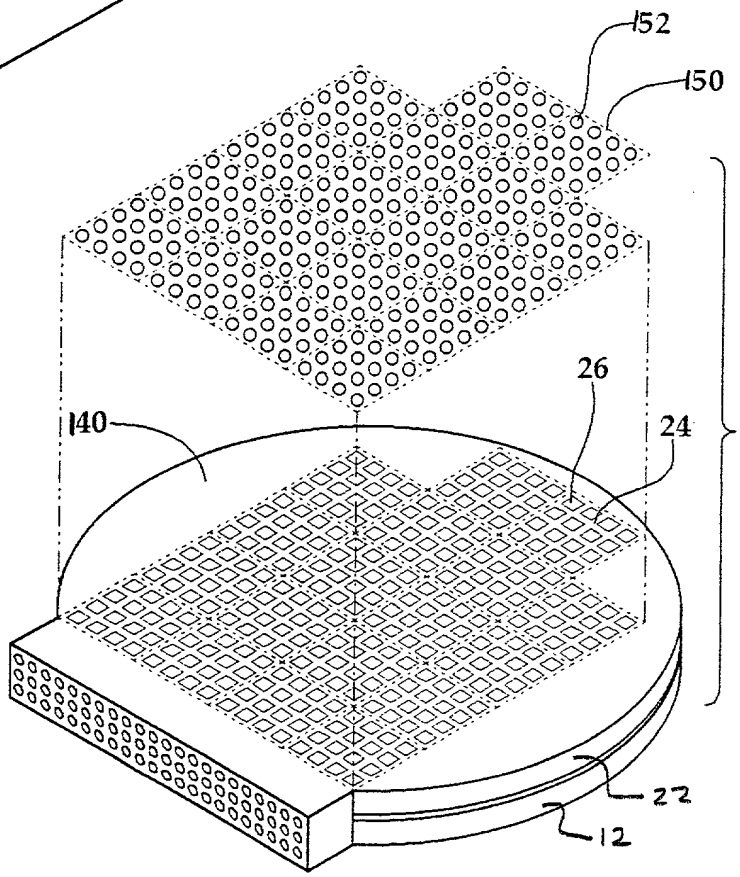

Fig. 14

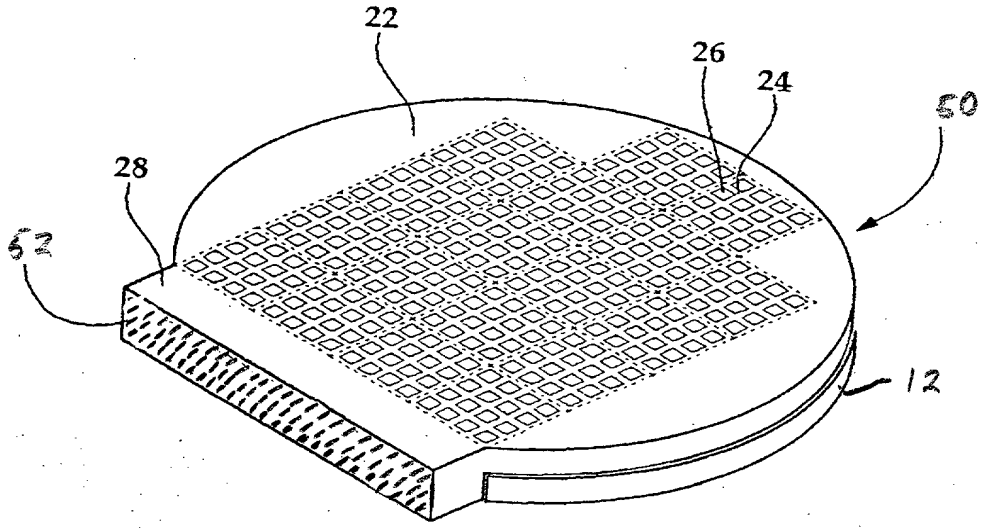

Fig 4.

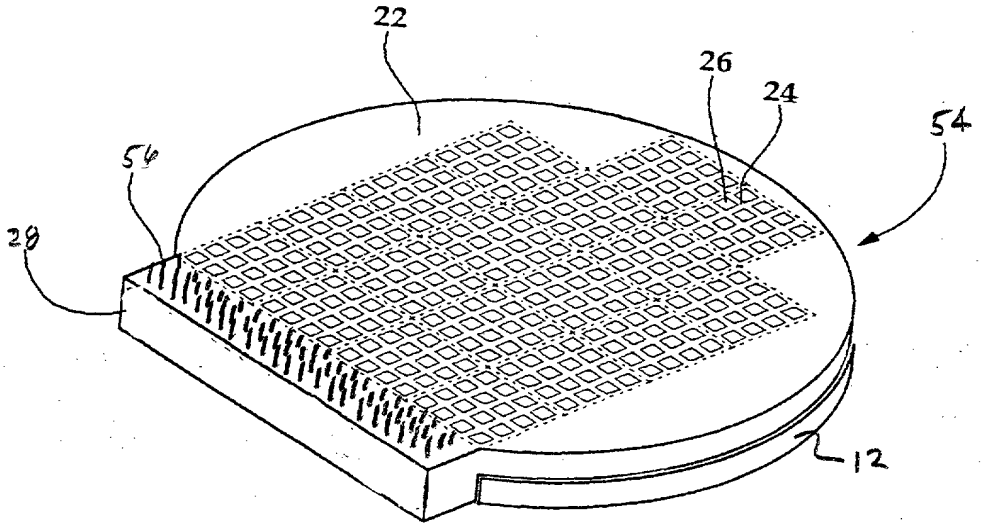

Fig. 5

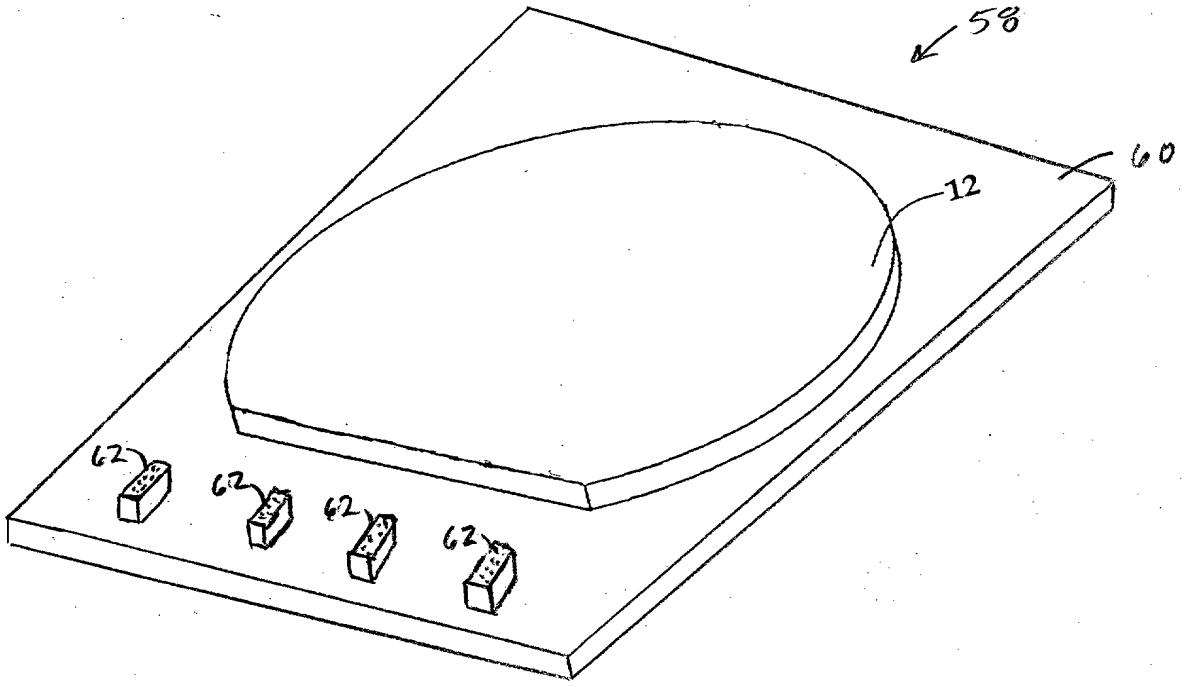

Fig 6

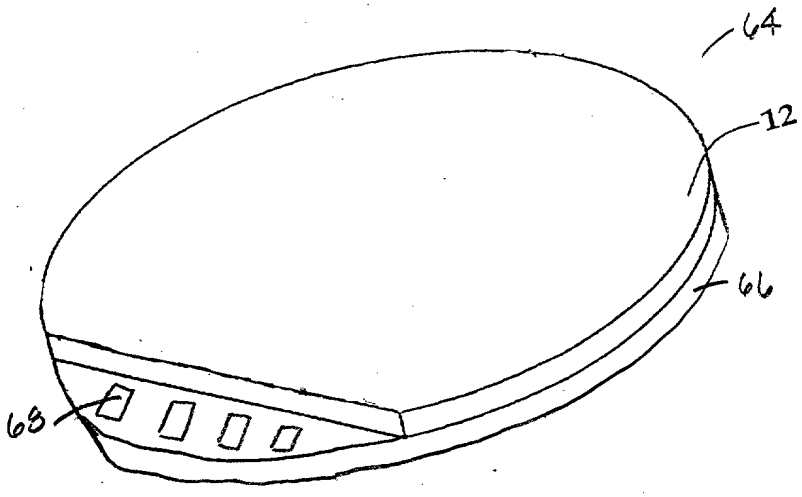

Fig 7

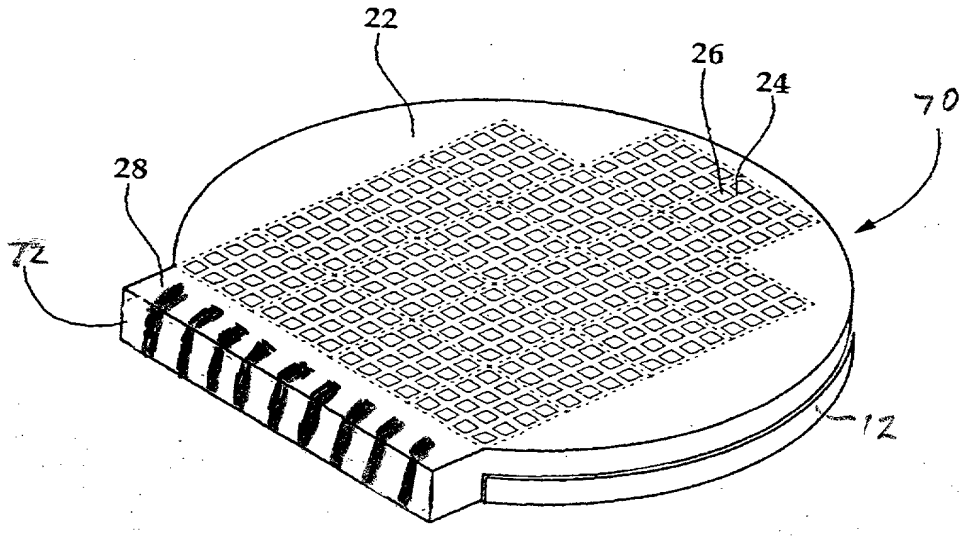

Fig 8

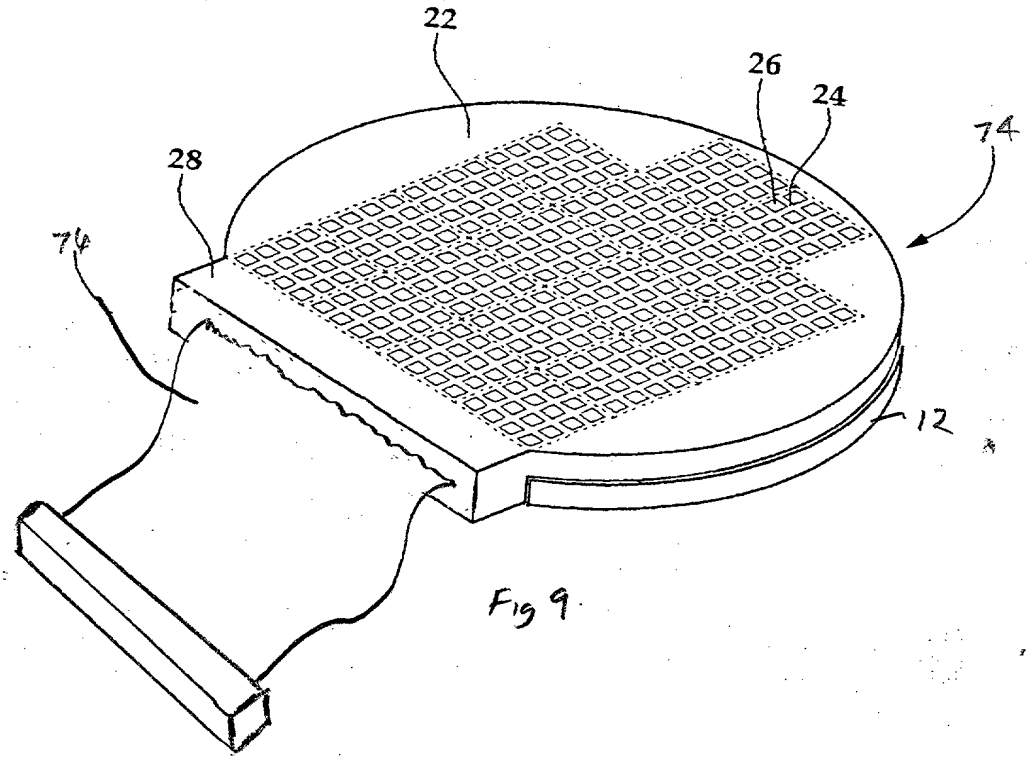

Fig 9

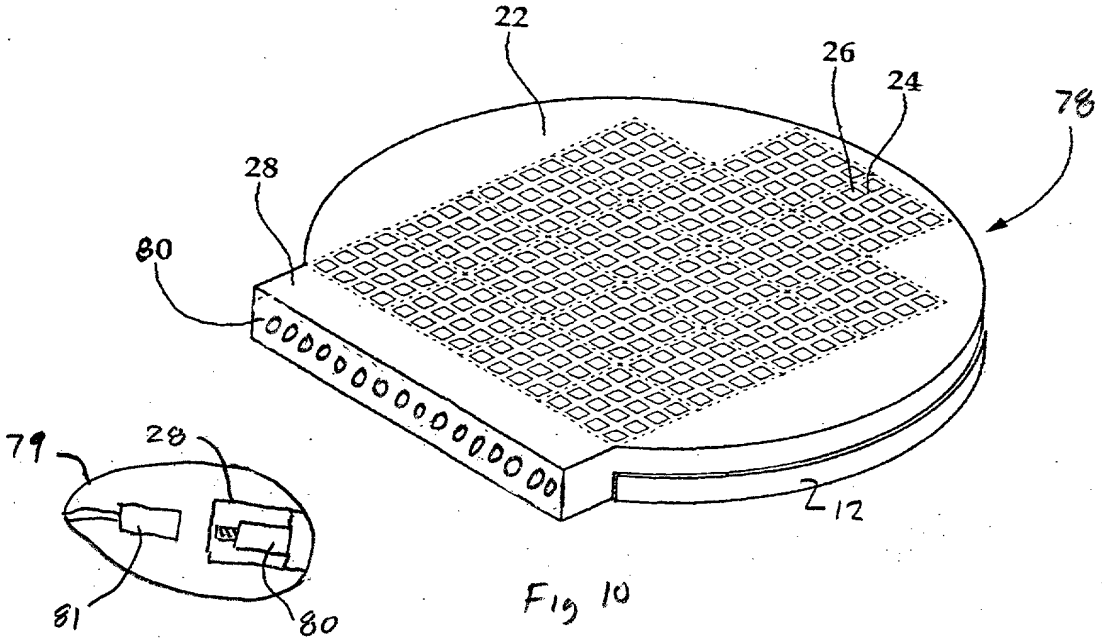

Fig 10

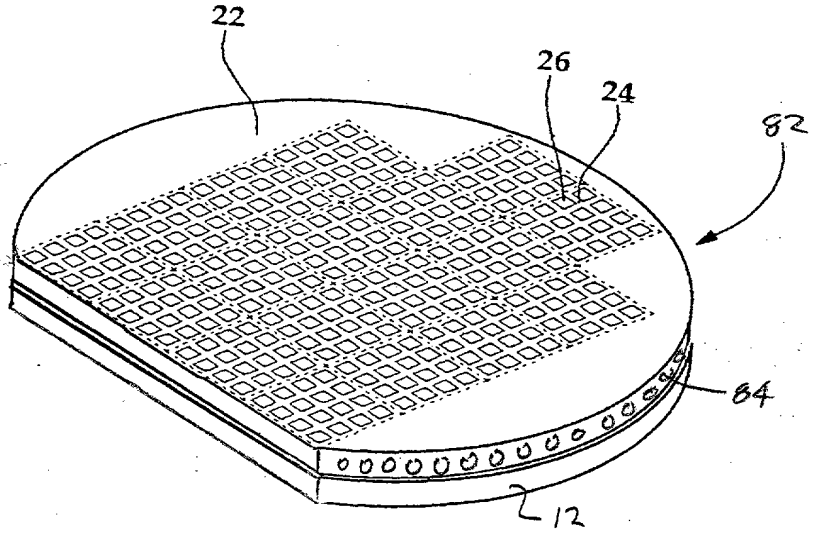

Fig 11

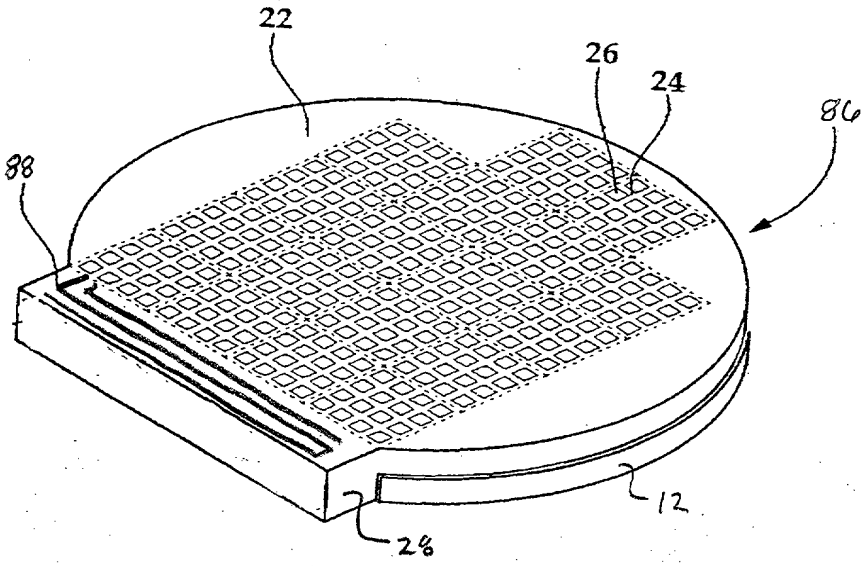

Fig 12

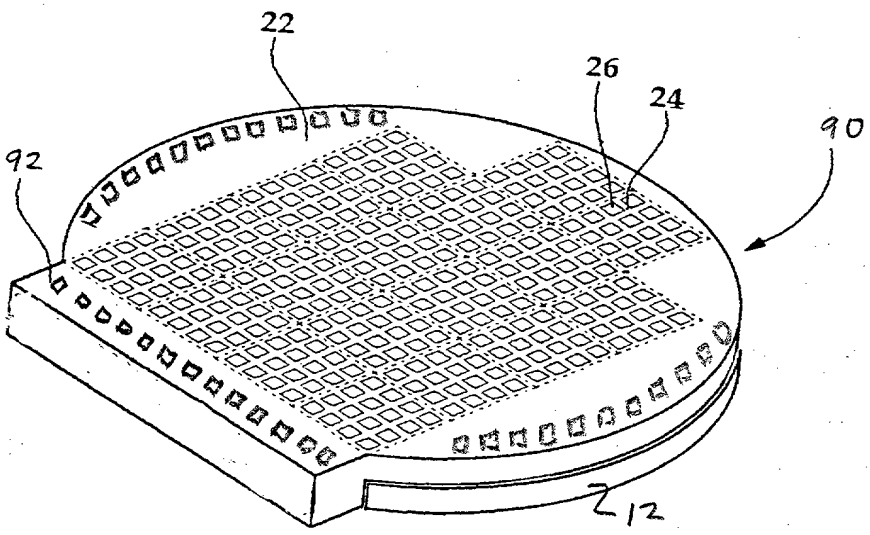

Fig 13

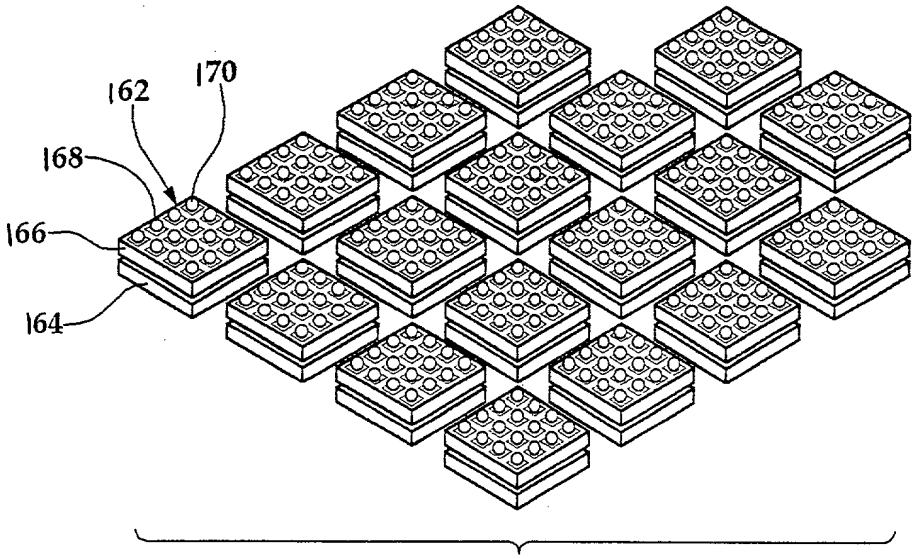

Fig. 15

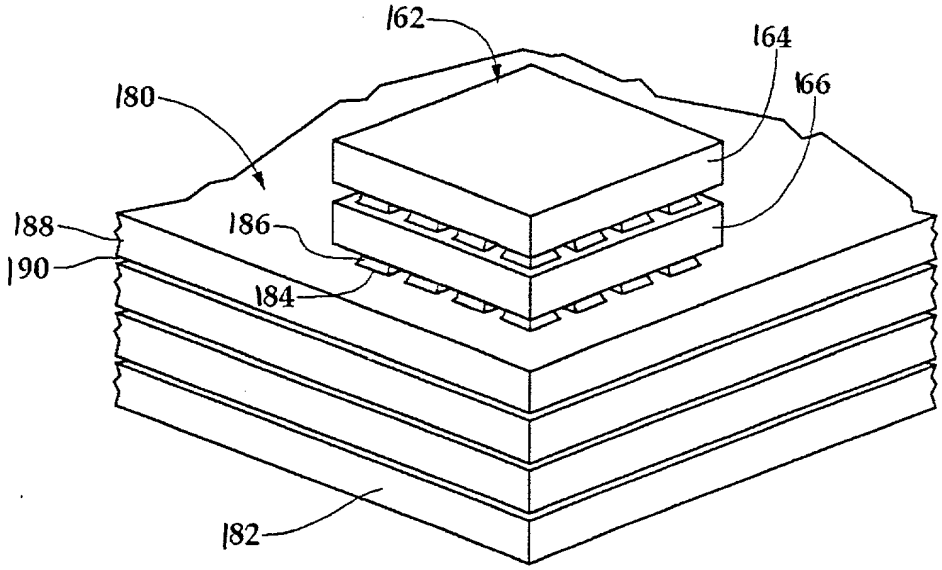

Fig. 16